Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Winter Examination-2015

Subject Name: ASIC Design

Subject Code: 5TE01ASD2 **Branch: M.Tech (EC)**

Semester: 1 **Date:29/12/2015** **Time: 10:30 To 1:30** **Marks: 70**

Instructions:

(1) Use of Programmable calculator and any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

SECTION – I

Q-1 **Attempt the Following questions** **(07)**

a. What is VHDL?
b. What is necessity of resolution function?
c. What is Package Body?
d. What is signal drivers?
e. What are Logical Operators?
f. What is function of EXIT statement?
g. What is function of NULL statement?

Q-2 **Attempt all questions** **(14)**

(a) List the major capabilities of VHDL along with the features that differentiate it from other hardware description languages.

(b) Discuss concurrent versus sequential signal assignment statement. What is the effect of Delta delay in VHDL?

OR

Q-2 **Attempt all questions** **(14)**

(a) Explain Inertial Delay model with suitable example. Also summaries effect of Inertial Delay on Signal Drivers. **8**

(b) Compare Signal and Variable in VHDL **6**

Q-3 **Attempt all questions** **(14)**

(a) Draw truth table for 8 X 3 encoder. Write VHDL code for 8x3 encoder Using: 1. If statement 2. When/else statement

(b) Explain Process statement. Explain the importance of sensitivity list. Quote suitable example.

OR

Q-3 **Attempt all questions** **(14)**

(a) Write a VHDL program for full Subtractor using structural modeling.

(b) Explain data types used in VHDL.

SECTION – II

Q-4 **Attempt the Following questions** **(07)**

a. Define Generics.

b. Define Default rules.

c. Define Signal attribute.

d. What is Programmable Logic Device?

e. What is necessity of resolution function?

f. What is Fuse?

g. What is Antifuse?

Q-5 **Attempt all questions** **(14)**

(a) Explain Component Instantiation.

(b) Briefly describe implicit and explicit visibility in VHDL.

OR

Q-5 **Attempt all questions** **(14)**

(a) Explain Configuration Declaration.

(b) Explain Subprogram Overloading.

Q-6 **Attempt all questions** **(14)**

(a) What is Test bench? Write typical Test Bench format.

(b) Discuss modeling of Mealy State Machine with suitable example

OR

Q-6 **Attempt all Questions** **(14)**

(a) Realize the following function using minimum row PLA.

$$F_1 = \sum m(2,3,5,7,8,9,10,11,13,15)$$

$$F_2 = \sum m(2,3,5,6,7,10,11,14,15)$$

$$F_3 = \sum m(6,7,8,9,13,14,15)$$

(b) Discuss modeling of Moore State Machine with suitable example.